Greg Tumbush, Ph.D., P.E.

Verification Expert

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Key Skills

AMS Verification
UVM Verification
SystemVerilog

Technical Skills

Cadence AMS
Synopsys CustomSim XA
Cadence Incisive/Xcelium

Education

University of Cincinnati
Ph.D. Computer Engineering
1998

Ohio State University
M.S. Electrical Engineering
1993

Wright State University
B.S. Electrical Engineering
1991, Cum Laude

Professional Profile

Recognized verification expert in UVM and Analog Mixed-Signal (AMS). Seventeen successful tape-outs spanning 20+ year career. Co-authored with Chris Speer, *SystemVerilog for Verification*, a top selling technical book.

Experience

Oct 2011 - Present
Digital Design/Verification Engineer • EM Microelectronic US
EM Microelectronic specializes in ultra low-power ASICs for consumer and medical markets.
Independently developed and verified:

- Mixed-signal ASICs using Cadence AMS and Synopsys CustomSim XA
- Real-Number models of analog blocks using Cadence AMS
- Digital logic using coverage driven UVM based test-benches
- RISCV based CPUs developed by OpenHW and internally

Led multi-site international verification teams
Key contributor on 9 successful tape-outs

Aug 2008 – May 2014
Instructor • University of Colorado, Colorado Springs
Created and instructed graduate courses in digital design methodology, verification using SystemVerilog and UVM, and rapid prototyping using FPGAs

Mar 2003-Oct 2011
Senior Digital Design Engineer • Starkey Labs/AMI Semiconductor/ON Semiconductor (multiple acquisitions)
ON Semiconductor specialized in low-power ASICs for medical market.

- Verified, using an object-oriented SystemVerilog test-bench, antenna capacitor matching ASIC for cell phone market
- Verilog design, verification with SystemVerilog, STA using PrimeTime, synthesis using DesignCompiler, and equivalency checking using LEC for glucose monitor ASIC with embedded ARM core; developed firmware to test ASIC
- Performed 100% of Verilog design, verification with SystemVerilog, STA using PrimeTime, synthesis using DesignCompiler, equivalency checking using LEC, and scan pattern generation using TetraMax for patient monitoring ASIC

Key contributor on 8 successful tape-outs

Feb 2000 – July 2002
Lead ASIC Design Engineer • Astek Corporation
Astek Corporation is a small company specializing in ASIC and FPGA design

- Designed and verified blocks using PCI, SCSI, AHB, and FiberChannel protocols
- Synthesized ASICs with Synopsys Design Compiler, analyzed timing with Synopsys Primetime, and equivalency checking with Conformal LEC

Mar 1993 – Sept 1994, Mar 1998-June 1999
Computer Engineer • US Air Force Research Lab

- Led technical effort to prove validity of accelerating DSP and graphics algorithms on FPGA-based reconfigurable computing platforms
- Designed DSP cores in VHDL, simulated using ModelSim, and synthesized with Synplify

References

Available upon request

Publications

See http://tumbush.com/published_papers/published_papers.html for publications.

Professional Organizations

- Technical program committee, Design and Verification Conference (DVCon), 2005-2007, 2009-present
- Co-Chair, North American SystemC Users Group (NASCUG), Summer