Greg Tumbush, Ph.D., P.E.
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Summary: 12 years experience in all aspects of ASIC and FPGA digital design from concept to fabrication.

QUALIFICATIONS

- Languages: Fluent in SystemVerilog**,** Verilog 2001, VHDL, SystemC, C/C++, Perl, Python, UNIX, and shell scripts.
- Designs: FLASH and PSBRAM memory controllers, Infiniband cores, PCI cores, ARM interfaces, FPGA emulation, low-power digital processor, low-power DSP algorithms, low-power wireless interface core, low-power CODEC. SystemC models of processor, memory management unit, etc.
- CAD Tools: Well versed in Synopsys's Design Compiler, Primetime, TetraMax, Power Compiler, and Formality tools as well as Cadence's Conformal, LogicVision, LSI Logic Flexstream, Synplify, ModelSim/QuestaSim, Exemplar, Signalscan, Verplex Conformal lec, Synopsys Formality, Xilinx, TransEDA Code Coverage, and Hspice tools.
- Bus Protocols: Highly knowledgeable of SPI, PCI-2.2, PCI-X, SCSI, FiberChannel, ARM High Speed Bus (AHB), Infiniband (IB), I^2C, and Compaq's Rapid Enabler for PCI-X (CREX) protocols.
- Team Leader: Managed small design teams on numerous successful projects.
- Circuit Theory: Well versed in fundamental circuit theory including architecture, logic design, layout, parasitics, timing and test.
- CAD Methodology: Extensive knowledge of design creation, synthesis, simulation, partitioning, place and route, code coverage, timing verification, equivalency checking, and testing.
- Communication and reporting: Managed financial and technical aspects of programs. Authored and presented technical papers at international conferences. Reviewed research proposals and VHDL book. Served on program committee of numerous conferences.

EMPLOYMENT HISTORY

Aug/08-Present Tumbush Enterprises, LLC, Owner

- Consulting company specializing in advanced digital design and verification in the medical ASIC industry.
- Digital Lead on patient monitoring ASIC tapeout. Performed all backend tasks (synthesis, static timing analysis, equivalency checking, scan pattern generation).
- Developed testbenches and wrote tests for hearing aid ASIC.

- Modified various blocks and performed all backend tasks except layout for a glucose monitor ASIC with an embedded ARM core. Wrote firmware to test ASIC.

Aug/08-Present University of Colorado, Colorado Springs, ½ time instructor
- Develop and instruct senior/graduate level courses in digital design methodology, verification using SystemVerilog, and rapid prototyping using FPGA's.

Mar/08-Aug/08 ON Semiconductor, Digital Design Engineer
- ON Semiconductor purchased AMI Semiconductor in '07
- More successful medical ASIC tapeouts.
- Expanded use of SystemVerilog methodology to include functional coverage and assertions using SVA.

July/06-Mar/08 AMI Semiconductor, Digital Design Engineer
- AMI Semiconductor purchased the Starkey Labs design center in July '06.
- Digital lead on numerous mixed signal medical ASIC's.
- Managed international teams of designers.
- Handled architecture, design, and verification.
- Implemented a SystemVerilog verification methodology for use in current and future projects.

March/03-July 06 Starkey Labs, Digital Design Engineer
Starkey is an international company specializing in the design and manufacture of hearing aids. The Colorado Springs office is Starkey's IC design center.
- Architected, designed and delivered on-schedule a very complex wireless interface module.
- Implemented a CODEC which included Wave Digital Filters, Sigma-Delta, and Pulse-Width Modulators, and slink filters.
- Explored architectures for CODEC using Synopsys Design Compiler and Power Compiler for minimum area/power.
- Architected and designed numerous blocks in SystemC.
- Developed a co-verification methodology for a DSP modeled in SystemC.
- Designed numerous blocks of the DSP in Verilog such as an interrupt controller, mathematical functions, debug controller, etc.
- Verified DSP using a combination of constrained random using the SystemC Verification Library (SCV) and directed tests.
- Achieved code coverage #'s in the 90th percentile using TransEDA's code coverage tools.
- Interviewed potential employees.
- Nominated for Performance Award in 2004

Feb/00-July/02 Astek Corporation, Lead ASIC Design Engineer
Astek Corporation is a small company specializing in the design of ASICs and FPGAs both in-house and on contract.

- Worked on nine major commercial projects.
- Extensively used Verilog in the creation of ASIC designs.
- Designed and verified blocks using PCI, SCSI, AHB, IB, and CREX protocols.
- Verified ASICs using FiberChannel and ATA protocols.
- Inserted BIST and JTAG into ASICs using LogicVision.
- Synthesized entire ASICs and cores with Synopsys Design Compiler.
- Analyzed timing with Synopsys Primetime.
- Prepared designs for fabrication in a LSI Logic process using their Flexstream 3.1 suite of CAD tools.
- Formally verified ASICs with Verplex Conformal lec.
- Wrote a PCI-X behavioral level model (BLM) in Verilog.
- Mentored junior engineers and managed small design teams.
- Adept at juggling multiple concurrent projects and quickly understanding new specifications and protocols.
- Recruited, interviewed, and recommended nine new employees.

March/98-June/99 Air Force Research Laboratory, Computer Engineer

- Led technical effort to prove validity of accelerating DSP and graphics algorithms on FPGA based reconfigurable computing platform.
- Designed DSP cores in VHDL, simulated using ModelSim, and synthesized with Synplify.
- Programmed Xilinx FPGAs with cores after placement/routing with Xilinx tools.
- Researched topics in design automation emphasizing partitioning algorithms.
- Managed $5 million in Air Force Research Laboratory programs with Synopsys, Inc., Lucent Technologies, and various subcontractors.
- Secret security clearance

March/93-Sept/94 Air Force Research Laboratory, Electrical Engineer

- Designed and verified a 0.35μm cell library.
- Began initial architecture definition of video processor to utilize cells.
- Secret security clearance

Jan/89-Sept/90 Central Intelligence Agency, Co-op Electrical Engineer

- Tested a wide range of analog and digital communications equipment for stock acceptance or field issue.
- Proficient in the use of laboratory test equipment such as function generators, spectrum analyzers, environmental test chambers, etc.
- Top Secret security clearance

EDUCATION

- **Ph.D. Computer Engineering**, March/98, University of Cincinnati, Dissertation Title – "Partitioning under Multiple Constraints", Focus: Design Automation
- **M.S. Electrical Engineering**, March/93, The Ohio State University,

Thesis Title – "Verification and Integration of a CMOS Process for CAD", Focus: VLSI Design and Computer Aided Design

- **B.S. Electrical Engineering**, June/91, Graduated Cum Laude, Wright State University, Focus: Digital Design

Publications

1. "Get to ASICs Faster - A Novel Mixed Signal Design Methodology", 2009 Design and Verification Conference (DVCon).
2. "SystemVerilog Tutorial", 2008 AMI Semiconductor Technical Forum.
3. "A 2mW 400MHz RF Transceiver SoC in 0.18um CMOS Technology for Wireless Medical Applications", 2008 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)
4. "Dramatically Increase the Performance of SystemC Simulations", 2007 Design and Verification Conference (DVCon).
5. "Dramatically Increase the Performance of SystemC Simulations", 2007 AMI Semiconductor Technical Forum.
6. "Signed Arithmetic in Verilog 2001 – Opportunities and Hazards", 2005 Design and Verification Conference (DVCon).
7. "Design and Verification of a Processor Using VHDL, Verilog, SystemC, and C++", 2004 Design and Verification Conference (DVCon). Won Best Paper Award
8. "Clustering to Improve Bi-Partition Quality and Run Time", 1999 IEEE International Symposium on Circuits and Systems (ISCAS).
9. "Partitioning under Multiple Constraints", 1998 PhD Dissertation.
10. "K-way Partitioning under Timing, Pin, and Area Constraints", 1997 IEEE International Conference on Innovative Systems in Silicon (ISIS)
11. "Partitioning Under Timing and Area Constraints", 1997 IEEE International Conference on Computer Design (ICCD)
12. "Development of a Deep Sub-Micron Standard Cell Library using the COMPASS Design Automation Tools" 1994 Compass Users Group Conference
13. "Verification and Integration of a Sub-Micron CMOS Process for CAD" 1993 Masters Thesis

Professional Organizations

1. Technical program committee Design and Verification Conference (DVCON), 2005-2007, 2009-2011
2. Co-Chair North American SystemC Users Group (NASCUG), Summer 2005/2006 and Spring 2006.